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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P5769	*Total Pages*	22
First Named Inventor or Application Identifier			
Gang Bai			
Express Mail Label No.	EM014063345US		

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

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1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 18]
(preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (*if filed*)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 CFR 113)* [*Total Sheets* 1]
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   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
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6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
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Note: Effective October 1, 1997.
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TOTAL AMOUNT OF PAYMENT ($) 790.00

Complete if Known	
Application Number	
Filing Date	06/30/98
First Named Inventor	Gang Bai
Group Art Unit	
Examiner Name	
Attorney Docket Number	042390.P5769

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1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790.00

2. CLAIMS

		Extra		Fee from below		Fee Paid
Total Claims	14	-20 =	0	X $22.00	=	0.00
Independent Claims	2	-3 =	0	X $82.00	=	0.00
Multiple Dependent Claims					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple Dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

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FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	400	216	200	Extension for response within second month	
117	950	217	475	Extension for response within third month	
118	1,510	218	755	Extension for response within fourth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,320	241	660	Petition to revive unintentionally abandoned application	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	
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Other fee (specify)					

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Typed or Printed Name	William Thomas Babbitt, Reg. No. 39,591			Reg. Number	
Signature	William Thomas Babbitt	Date	6/30/98	Deposit Account User ID	02-2666

Attorney's Docket No. 042390.P5769
Express Mail No. EM014063345US

UNITED STATES PATENT APPLICATION

FOR

A MULTI-LAYER GATE DIELECTRIC

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BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to integrated circuit devices and more particularly to enhancing dielectric material in those device.

Description of Related Art

One way to improve integrated circuit performance is through scaling the individual devices that comprise the integrated circuit. Thus, each subsequent generation of integrated circuit generally involves reducing the size of the individual devices on, for example, a semiconductor chip. The Morse rule is a common benchmark in the integrated circuit technology and provides that devices will be scaled down or reduced in size by one-third for each new generation.

The scale of a transistor device requires consideration of the desired performance of the device. For example, one goal may be to increase the current flow in the semiconductor material of the transistor. The current flow is proportional to the voltage applied to the gate electrode and the capacitance seen at the gate:

$$Q \propto C(V-V_{th})$$

where Q is one measure of the current flow, C is capacitance, V is the voltage applied to the gate electrode, and V_{th} is the threshold voltage of the device.

To increase the voltage applied to a device requires an increase in power, P ($P \propto V^2$). However, at the same time as increasing the charge in the transistor, subsequent generations also seek to reduce the power required to run the device, since, importantly, a reduction of power reduces the heat generated by the device. Thus, to increase the current flow through the device without increasing the power requires an increase in the capacitance in the gate.

One way to increase the capacitance is by adjusting the thickness of the gate dielectric. In general, the capacitance is related to the gate dielectric by the following formula:

$$C = k_{ox}/t_{electrical}$$

where k_{ox} is the dielectric constant of silicon dioxide (SiO_2) and $t_{electrical}$ is the electrical thickness of the gate dielectric. The electrical thickness of the gate dielectric is greater than the actual thickness of the dielectric in most semiconductor devices. In general, as carriers flow through the channel of a semiconductor-based transistor device there is a quantum effect experienced in the channel which causes an area directly below the gate to become insulative. The insulative region acts like an extension of the gate dielectric by essentially extending the dielectric into a portion of the

channel. The second cause of increase gate dielectric thickness attributable to $t_{electrical}$ is experienced by a similar phenomenon happening in the gate electrode itself. At inversion, a gate electrode of polysilicon, for example, will generally experience a depletion of carriers in the area of the polysilicon near the gate dielectric. Accordingly, the gate dielectric appears to extend into the polysilicon gate electrode.

The result of the quantum effect in the channel and a depletion in the polysilicon gate electrode is an electrical thickness ($t_{electrical}$) of the gate dielectric greater than the actual thickness of the gate dielectric. The magnitude of the channel quantum effect and polysilicon depletion may be estimated or determined for a given technology. Accordingly, the electrical thickness ($t_{electrical}$) for a SiO_2 may be calculated and scaled for a given technology.

In considering the capacitance effects of the gate dielectric, a consideration of the thickness of gate dielectric is important for other reasons. First, the gate dielectric cannot be too thin as a thin gate dielectric will allow a leakage current from the channel through the gate electrode. At the same time, the gate dielectric cannot be too thick because such a gate structure may produce an undesirable fringe electric field. The desired electric field at the gate is typically perpendicular to the surface of the semiconductor substrate. Beyond a certain gate dielectric thickness, generally thought to

be beyond one-third the lateral width of the gate electrode for a SiO_2 gate dielectric, the electrical field deviates from a perpendicular course and sprays about the gate electrode leading to an undesirable fringe electric field.

What is needed is a way to increase the capacitance of a gate dielectric without decreasing the performance of the device. It is preferable if the increased capacitance is consistent with scaling techniques and may be used in multiple generation technologies.

SUMMARY OF THE INVENTION

A transistor gate dielectric is disclosed. The transistor gate dielectric includes a first dielectric material having a first dielectric constant and a second dielectric material having a second dielectric constant different from the first dielectric constant.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic illustration of a side view of a transistor dielectric having a gate dielectric of a first dielectric material and a second dielectric material.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates to a transistor gate dielectric made up of at least two different dielectric materials. For example, one embodiment contemplates a gate dielectric made up of two different dielectric materials each with its own dielectric constant. The dielectric material nearest the substrate, e.g., a semiconductor substrate will have a modest dielectric constant that produces a defect-free interface with the substrate and is stable against oxide formation. The second dielectric material will have a relatively high dielectric constant and be stable in contact with the desired gate material. By varying the thickness of the material, a gate dielectric can be formed that is scalable for different technology generations, has a low leakage current, and maintains an electric field of the gate perpendicular to the surface of the semiconductor. A transistor gate utilizing the multi-layer gate dielectric is also disclosed.

Figure 1 illustrates an embodiment of the multi-layer gate dielectric of the invention. Figure 1 shows transistor 100 consisting of gate electrode 110 overlying gate dielectric 140. Gate electrode 110 and gate dielectric 140 overlie semiconductor substrate 105 such as, for example, a silicon semiconductor substrate. Formed in substrate 105 adjacent transistor gate electrode 110 are diffusion or junction regions 160. The

transistor is isolated from other devices, in this example, by shallow trench isolation structures 150.

Gate dielectric 140 is made up of, in this example, a bi-layer gate dielectric stack. The gate dielectric material is deposited by conventional techniques such as chemical vapor deposition or other deposition techniques according to the specifics of the material. The individual dielectric materials that make up the gate dielectric stack are patterned using conventional techniques such as masking and etching.

In one embodiment, the bottom dielectric layer 130 is selected to have a modest dielectric constant, k_1, that forms a generally defect-free interface with substrate 105. A generally defect-free interface is one that has a sufficiently high (e.g., >8 MV/cm) dielectric breakdown strength implying that the dielectric layer is pin-hole free and contains a negligible number of defects that would lead to breakdown of the dielectric layer at lower electric fields. Bottom dielectric layer 130 should also be stable on silicon and stable against oxide formation. In one embodiment, bottom dielectric layer 130 materials are chosen that have a heat of formation greater than the heat of formation of SiO_2. The chemistry in terms of stability of bottom layer 130 is important to achieve the low defect interface. Examples of suitable bottom dielectric layer 130 include, but are not limited to, hafnium oxide (HfO_2), zirconium oxide (ZrO_2), barium oxide (BaO), lanthanum oxide (La_2O3), and yttrium oxide (Y_2O_3).

In this embodiment, top dielectric layer 120 is selected to have a relatively high dielectric constant, k_2, and is a material that is stable in contact with gate electrode 110. Examples of suitable top dielectric layers are $BaSrTiO_3$ (BST) and $PbZrTiO_3$ (PZT). One function of top dielectric layer 120 is to block any leakage current through bottom dielectric layer 130, without adding to the equivalent thickness of gate dielectric 140 (i.e., equivalent thickness of an SiO_2 gate dielectric) and contributing to the production of a fringe electric field.

One guideline to select the appropriate dielectric layer thickness t_1 for bottom dielectric layer 130, and t_2 for top dielectric layer 120, is the following. For a given technology generation (i.e., a given gate length of gate electrode 110 and equivalent oxide thickness of a SiO_2 gate dielectric, t_{ox}), a total thickness, t, of gate dielectric 140 should be less than one-third of the gate length of gate electrode 110. The effective dielectric constant, k, may then be determined by the following relationship:

$$k = k_{ox} \, (t/t_{ox}) \qquad (1)$$

wherein k_{ox} is the dielectric constant of SiO_2 which is typically represented as 4.0.

Combining the above relationship with a relationship for calculating the effective dielectric constant of gate dielectric 140 of the following:

$$k = t/(t_1/k_1 + t_2/k_2), \quad (2)$$

the total thickness of dielectric layer 140 may be calculated:

$$t = t_1 + t_2. \quad (3)$$

Combining equations (1), (2), and (3) yields the following:

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}. \quad (4)$$

Equation (4) is then solved for a thickness of bottom dielectric layer 130 having a known dielectric constant, k_1, and top dielectric layer 120 also having a known dielectric constant, k_2. Table I shows the individual thicknesses of first dielectric layer 130 (t_1) and second dielectric layer 120 (t_2) for various technologies scaled by the Morse rule starting with a gate electrode length of 150 nanometers, for a k_1 of 30 and a k_2 of 300.

Table I demonstrates that a multi-layer dielectric gate stack, in this case, a bi-layer dielectric gate stack, is scalable for a given technology. For example, for each technology, given a first dielectric layer 130 having a dielectric constant k_1 of 30 and a second dielectric layer 120 having a dielectric constant k_2 of 300, a total gate dielectric layer thickness less than one-third of the individual gate lengths is maintained. Further, the choice of second gate dielectric layer 120 of material to block the leakage current maintains the performance of the device. Finally, by manipulating the gate dielectric materials, the capacitance of

the device may be appropriately increased for the given technology.

For a gate electrode 110 that is polysilicon, a third dielectric layer may be utilized to act as a barrier layer to prevent interaction between top dielectric layer 120 materials having high dielectric constants and the polysilicon gate material. Suitable third dielectric materials include, but are not limited to, HfO_2, ZrO_2, BaO, La_2O_3, and Y_2O_3 (notably the same materials suitable as bottom dielectric layer 130).

The above example is described with respect to gate electrode 110 being a polysilicon. It is to be appreciated that the same principles may be applied to gate electrodes of different materials, such as, for example, metal gates. In the case of a metal gate electrode, the electrical thickness ($t_{electrical}$) may be reduced since, in general, metal gate electrodes do not experience the depletion seen by polysilicon. Table I also shows the scaling of the bi-layer dielectric materials discussed above using metal gate technology.

Technology Generation	1	2	3	4	5	6
Lgate (nm)	150	100	70	50	35	25
t_electrical (Å)	30	21	15	10	7	5
t_ox (Å):metal gate	26	17	11	6	3	1
t (Å):total stack thick	300	210	147	103	72	50
t_1 (Å), k_1=30	183	118	75	39	17	3
t_2 (Å), k_2=300	117	92	72	64	55	48

Table I

In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed:

1. A transistor gate dielectric comprising:

a first dielectric material having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant.

2. The transistor gate dielectric of claim 1, wherein the second dielectric constant is greater than the first dielectric constant.

3. The transistor gate dielectric of claim 1, wherein the first material has a first thickness and the second material has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of the length of a transistor gate adapted to overly the gate dielectric.

4. The gate dielectric of claim 3, wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

5. The gate dielectric of claim 1, wherein the first gate dielectric material is selected from one of silicon nitride, HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2.

6. The gate dielectric of claim 1, wherein the second dielectric material is selected from one of BST and PZT.

7. The gate dielectric of claim 1, further comprising a third dielectric material having a third dielectric constant.

8. A transistor having a gate electrode overlying a gate dielectric comprising:

a first dielectric material having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant.

9. The transistor of claim 8, wherein the second dielectric of the gate dielectric has a dielectric constant greater than the first dielectric constant.

10. The transistor of claim 8, wherein the first material of the gate dielectric has a first thickness and the second material of the gate dielectric has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of a length of the transistor gate electrode.

11. The transistor of claim 8, wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate electrode length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

12. The transistor of claim 8, wherein the first gate dielectric material is selected from one of silicon nitride, HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2.

13. The gate dielectric of claim 8, wherein the second dielectric material is selected from one of BST and PZT.

14. The gate dielectric of claim 8, further comprising a third dielectric material having a third dielectric constant.

ABSTRACT OF THE DISCLOSURE

A transistor gate dielectric including a first dielectric material having a first dielectric constant and a second dielectric material having a second dielectric constant different from the first dielectric constant.

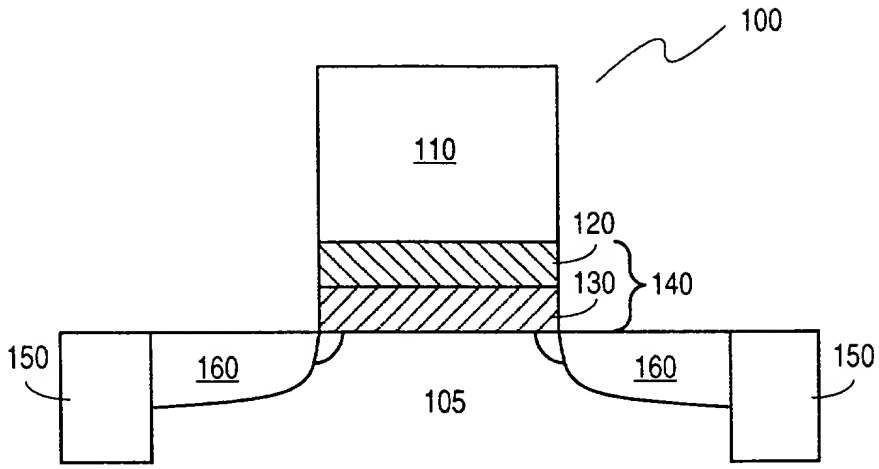

Fig. 1

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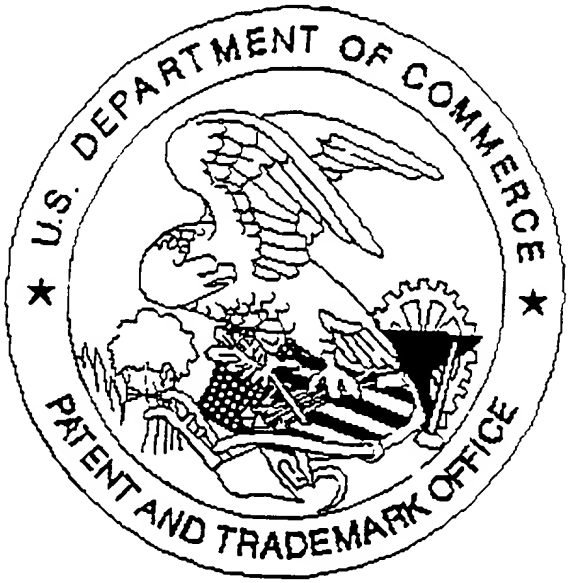

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